# Status of Run 2b Silicon

*Joe Incandela*

*University of California, Santa Barbara*

*CDF Run 2b Silicon Group Leader*

*Fermilab PAC Meeting*

*April 22, 2001*

# Outline

- General Considerations
- Physics
- Basic Plan
- Project Status
- Schedule & Cost

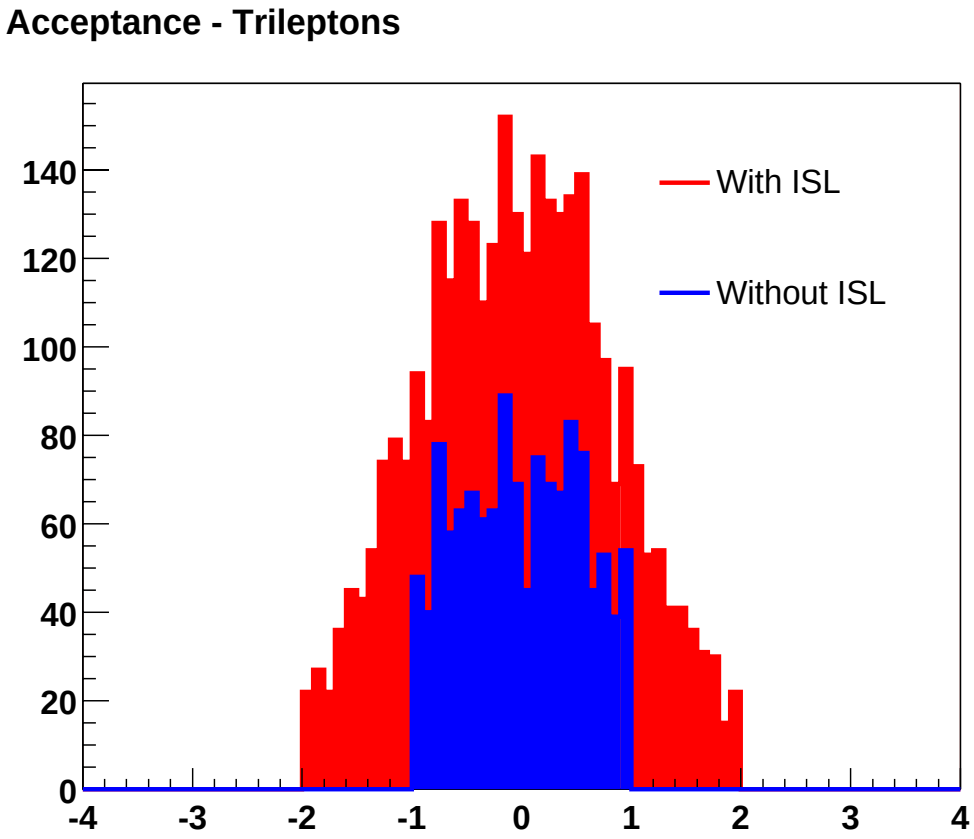
# General Considerations

- Longevity
  - The Run 2a Silicon detector cannot be guaranteed to last 15 $fb^{-1}$
    - We will monitor the detector carefully to better understand the lifetimes of each layer (covered in more detail below).
- Scale
  - We are preparing to build a replacement for Layer 00 and SVXII
    - There is no other sensible option
- Primary Goals
  - Retain current capabilities with a more robust and simple system
    - This will also help us to meet our schedule
- Secondary Goals
  - Enhance performance
    - Where possible without significant schedule risk or added cost.

# Silicon Tracking

- Silicon is a key tracking device in CDF
  - In the region $1 \leq |\eta| \leq 2$ silicon is our only tracking.
    - Impaired performance at large radius would mean
      - Loss of robustness and track purity
      - Loss of momentum resolution (which also degrades impact parameter info.)
      - Loss of extrapolation to end cap calorimeters would limit lepton coverage.
    - Impaired performance at small radius would mean
      - Loss of impact parameter resolution and b tagging degradation
    - Impaired performance at any radius
      - Loss of a track constraint which affects track purity.
  - Tracking improves jet energy measurements

# Physics




- Higgs and SUSY sensitivity depends mainly on 3 things:
  - B Tagging
    - For W/Z+H, H $\rightarrow b\bar{b}$ the ability to tag b jets in $1 \leq |\eta| \leq 2$ increases acceptance in this channel by 70%. For ttH the acceptance increase is even larger.
    - High b tag efficiency is only relevant if tagging is pure.
      - minimize light quark, gluon jet tags
      - distinguish charm from bottom
  - Lepton id
    - For SUSY channels with 3 leptons the ability to track and determine particle momenta in $1 \leq |\eta| \leq 2$ accounts for the majority of our sensitivity.
  - Energy resolution
    - Jet energy and missing $E_T$ resolution need to be optimal.

# Run 2a Performance Issues

- Material
  - Could impair standalone silicon tracking.
    - Loss of even one layer of SVXII significantly increases the fake rate for SVXII track primitives. (1996 TDR track studies).
- Stereo
  - Ambiguities in 90 degree layers increase inversely with radius
  - Stereo IP resolution is not very comparable to axial resolution
- Resolution
  - Substantial fraction of tracks in high energy b jets merge in L00
    - Degrades IP resolution

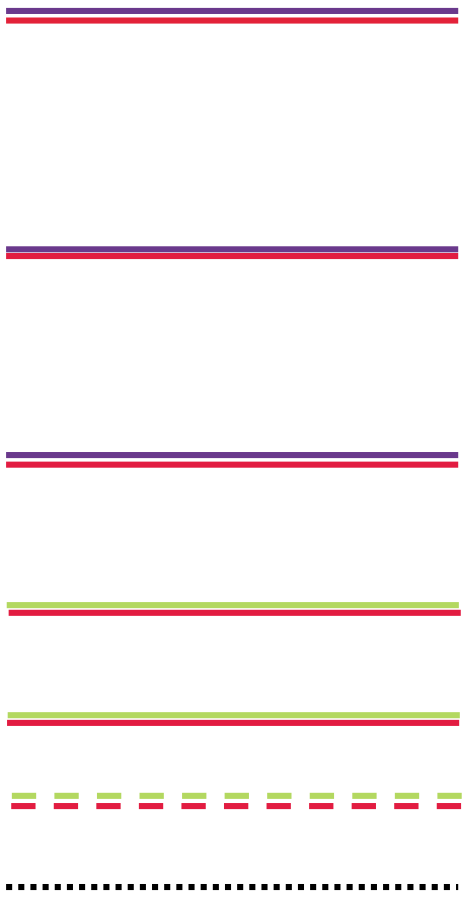
# Basic Plan

- Replace SVXII and Layer 00
  - 6 new axial layers
  - 2-3 90° stereo layers
  - 3 1.2° stereo layers
- Simplify for speed & cost
  - Single-sided (SS) silicon & hybrids
    - Easier to procure at lower cost
  - No hybrids mounted on silicon
    - Simpler module fabrication, fewer electronics/noise issues.
  - Universal types
    - 2 hybrid types instead of 12
    - Minimum number of ladder types
  - Increase radial spread of layers
    - Greatly simplifies mechanical supports and assembly
  - No optical components in DAQ
    - Reduces power consumption and cooling needs
  - No beryllium bulkheads
    - Eliminates a costly, long lead time item
- Automatic Improvements
  - Material in tracking region
    - No port cards (~4% $X_o$)
    - No hybrids (~1.5 % $X_o$ per layer)
  - More uniform radial distribution
    - No large gap between ISL and next innermost layer
    - Additional layer near ISL provides a strong standalone tracking anchor
  - Increased Acceptance
- Also under consideration
  - small radius 90° layer

# Progress & Plans

- Work in Progress
  - Layout & performance
  - Mechanics & cooling
  - Chips & Hybrids
  - DAQ & Power Supplies
  - Silicon & Lightweight cables
- Planning
  - Organization
  - R&D/Prototyping
  - Performance studies & Finalizing the design
  - Radiation monitoring
  - Schedule & Cost

# Layout: Current thoughts*




- Outer region: Tracking group
  - 3 layers made up of Axial + Shallow stereo ($1.2^o$ – $2.5^o$)
  - 1.2 m long
  - optimizing strip length & stereo angle
  - 50/100 μm pitch/readout
  - Operate silicon at 0-10 C
- Inner region: Optimizing now
  - Two $0^o$/$90^o$ layers
    - intermediate strips
    - Smaller pitch
    - 0.8 m long
  - High resolution layer
    - Layer 00 replacement
    - $90^o$ layer under study
  - Silicon must be kept cold (–10 C)
- Run 2b versus Run 2a

  2 vs 12 hybrid designs

  4 -6 vs 12 silicon masks

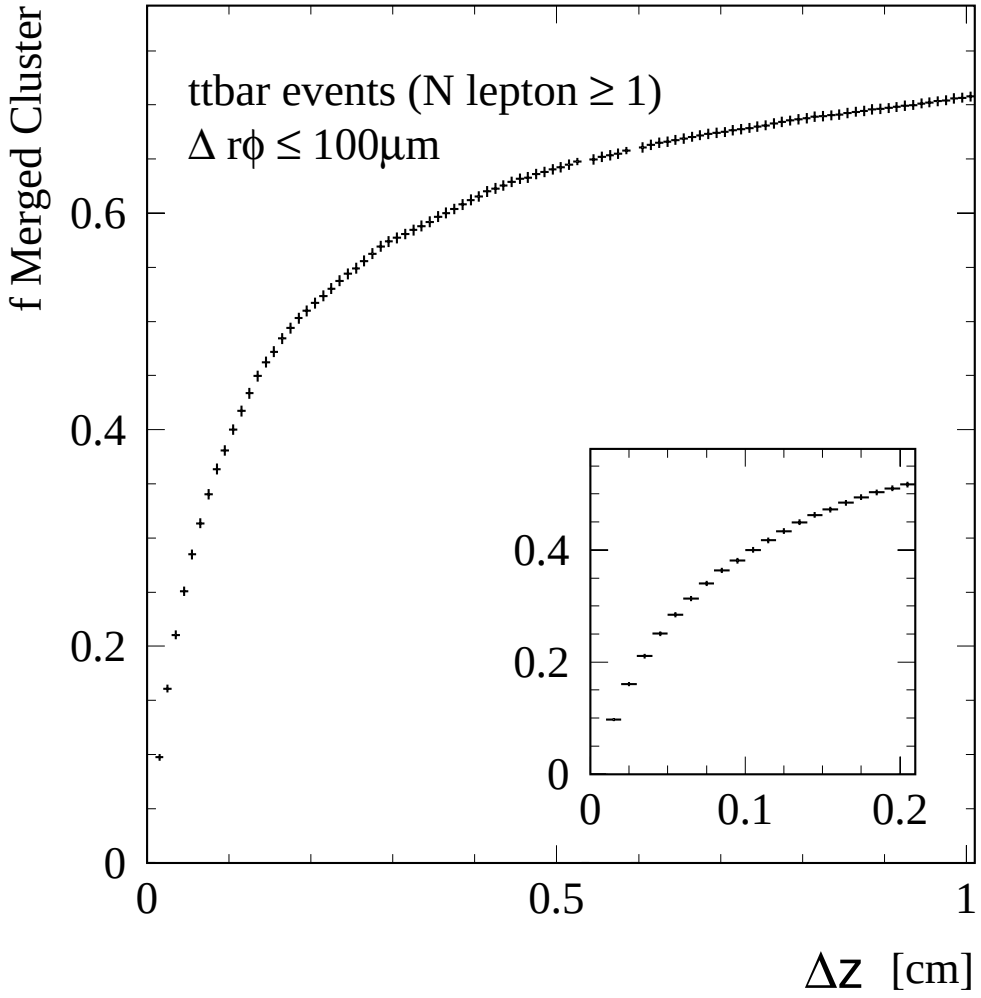
* under study…

# Layout Performance

- Outer layers
  - provide reasonable layer hit resolution
    - $\sigma_z$ ~ 500 μm, $\sigma_\phi$ ~ 15 μm
  - Combined with ISL to provide good pointing into inner layers
    - $\sigma_z$ ~ 500 μm, $\sigma_\phi$ ~ 15 μm at a radius of 5 cm
  - Combine with ISL for high purity
    - 3 large radius layers have been shown to be a powerful seed for tracking
      - Particularly useful in high luminosity environment
    - 5 total layers of shallow stereo provide relatively robust pattern recognition
- Inner group
  - Axial layers in the SVT
  - Good focus of z tracking
    - Pointing to 2nd layer ~60 μm, pointing to 1st layer ~30 μm
  - Stereo IP resolution closer to axial IP resolution
    - $\sigma_z$ ~ 20 μm, $\sigma_\phi$ ~ 7 μm
- Material

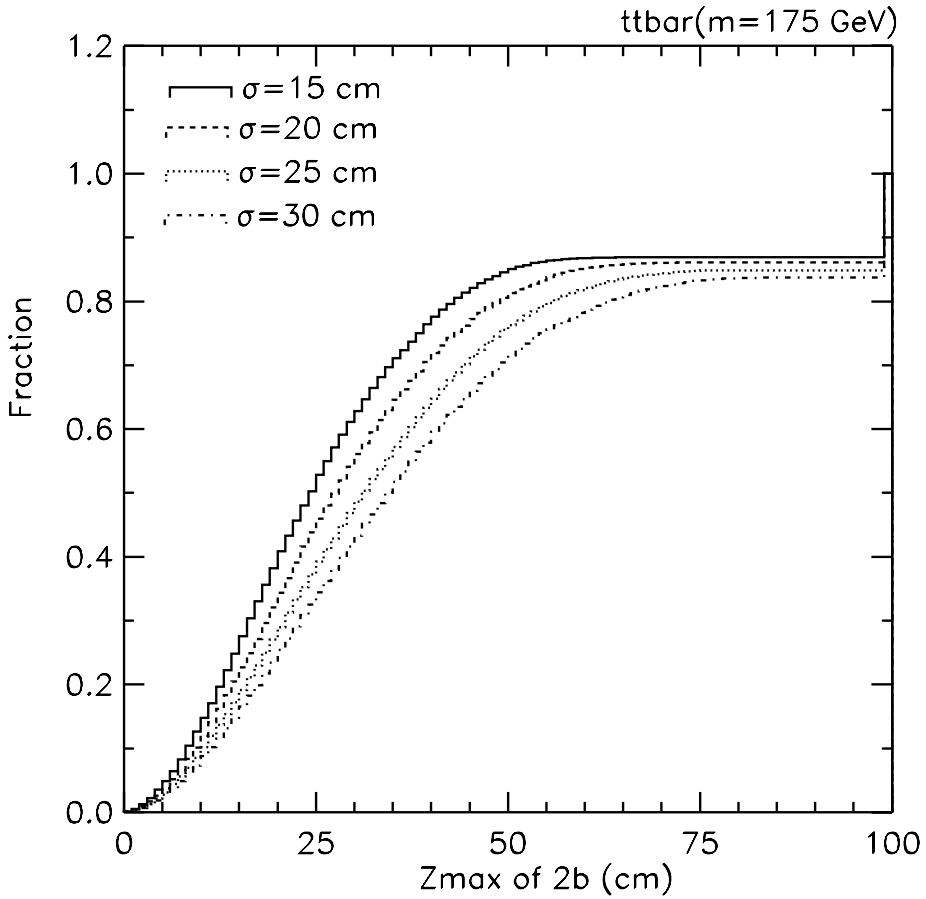
  x2 material reduction in the tracking region.

# 3D Versus 2D




- Beneficial to physics
  - Separation of hits which are merged in Layer 00
    - In high energy b jets up to 30% of b daughter hits are merged
    - less than 10% of these hits are closer than 250 μm in z (see figure).
  - Could improve purity and efficiency

# Acceptance

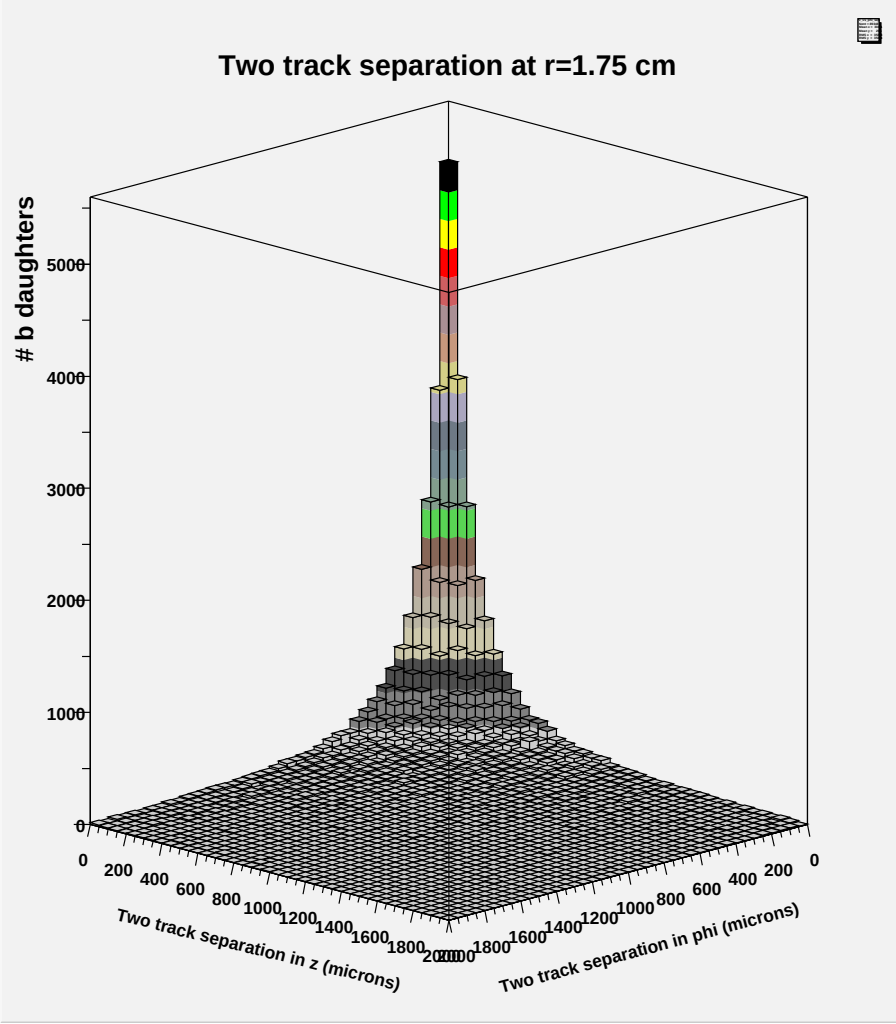


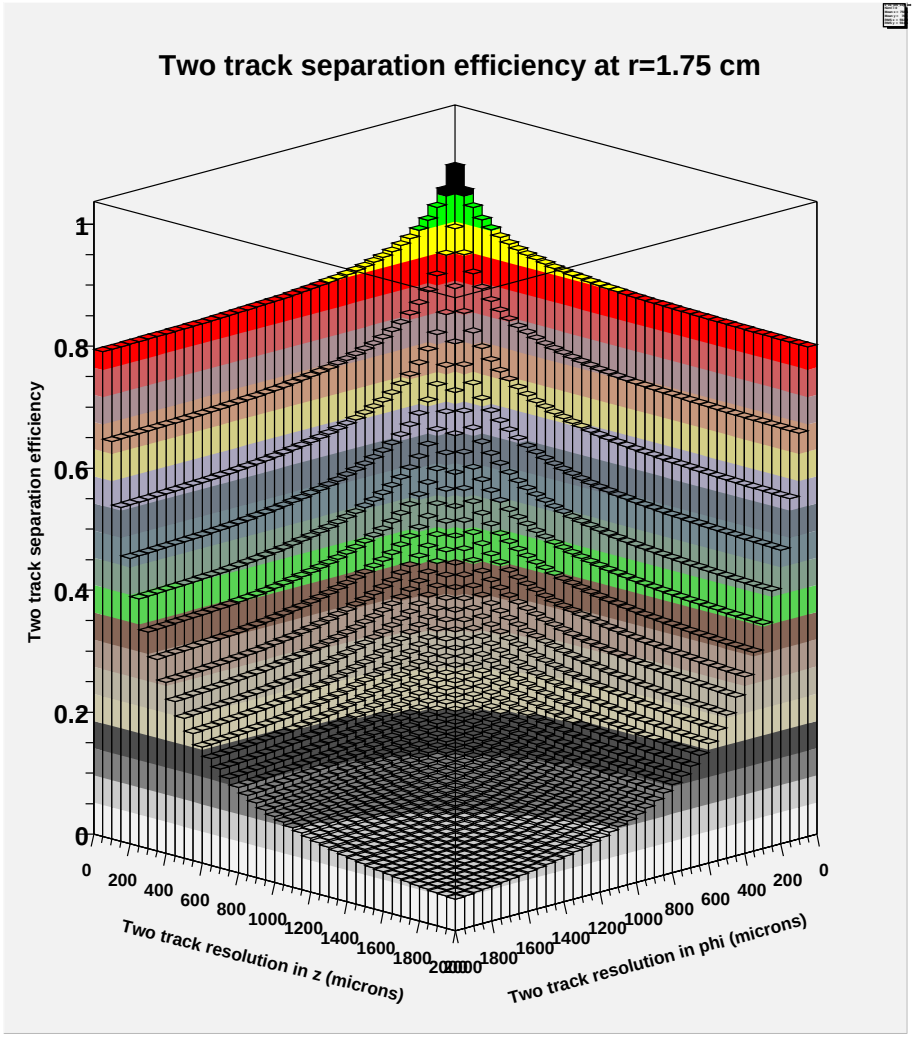

- Luminous region ("$\sigma_z$")
  - ➤ Run 2a: $\sigma$ ~ 30 cm
  - ➤ Run 2b: Smaller w/crossing angle
- Impact on physics
  - ➤ Retain or increase 'length'
    - Acceptance for second taggable b jet in top increases from ~70% to 89% (25% relative increase)
    - ~ same improvement for WH
    - ~ double this for Htt
- Impact on cost
  - ➤ Retain current $\eta$ coverage
    - Little or no savings in Silicon cost
    - Some few % savings elsewhere

# Studies in Progress

- Study grouped formed – meeting weekly
  - Short term: “Parametric” studies
    - 3D impact parameter resolutions
    - pointing resolutions (linking of different radial groups)
    - as a function of radius
      - track density and overlaps
      - ghosting versus shallow stereo angle & strip length
  - Medium Term: Material modeling
    - Fully model the detector in Run 2 framework
      - secondary production
      - tracking
  - Physics (for TDR this fall)
    - Benchmark modes (WH,ZH,ttH,SUSY)

# Optimization

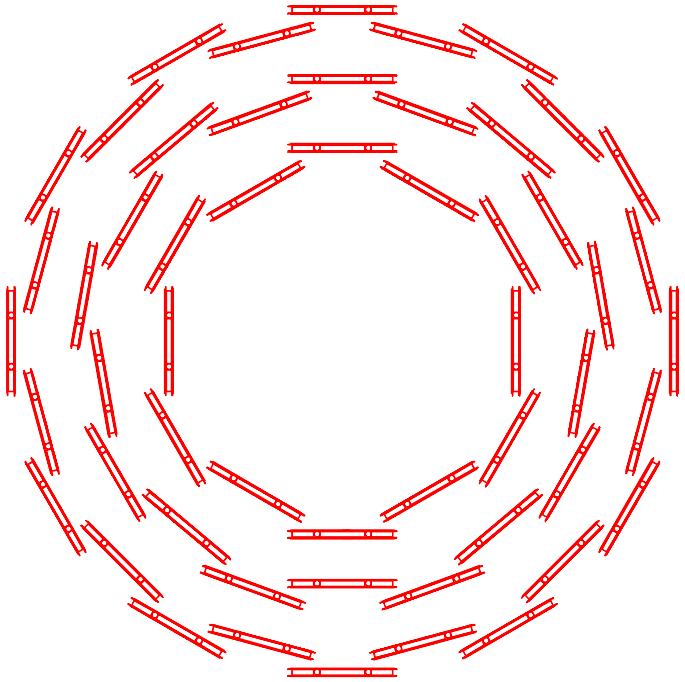


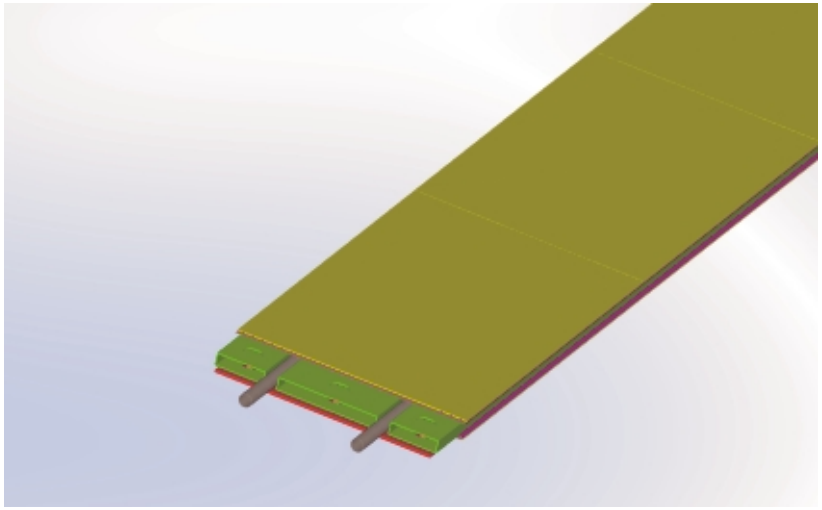



# Mechanics

- CERN Visit: G.Derylo, M.Hrycyk, R.Plunket, P.Tipton, and J.Incandela
  - Extensive tours in mid-January
    - CMS engineering and prototyping work for the CMS silicon tracker
    - ATLAS engineering and prototyping work for pixels
  - Learned a lot about materials, cooling concepts etc.
    - CMS will use $C_6F_{14}$ which allows them to cool to –25 C
      - maybe something we should at least consider ?
    - ATLAS pixels taught us that cooling is a major consideration.
      - 5 years of R&D on two phase cooling system at CERN
      - Beautiful low-mass, self-regulating system.
- UCSB involvement: D.Hale and S.Kyre have joined the design team.
  - Valuable Babar & CLEO low-mass, high precision mechanics experience.
- Current activities:
  - Meet bi-monthly with Mike Hyrcyk and a small handful of top experts from CDF silicon community
    - Converging fast on simple, easy to build mechanical designs
    - Established the relevant ranges of possibilities for specifications

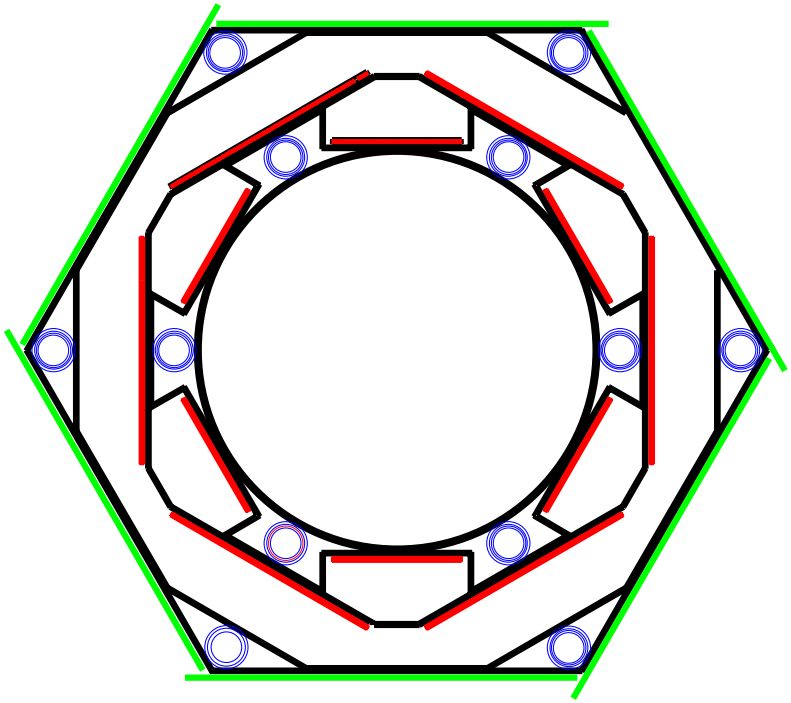
# Outer Layers





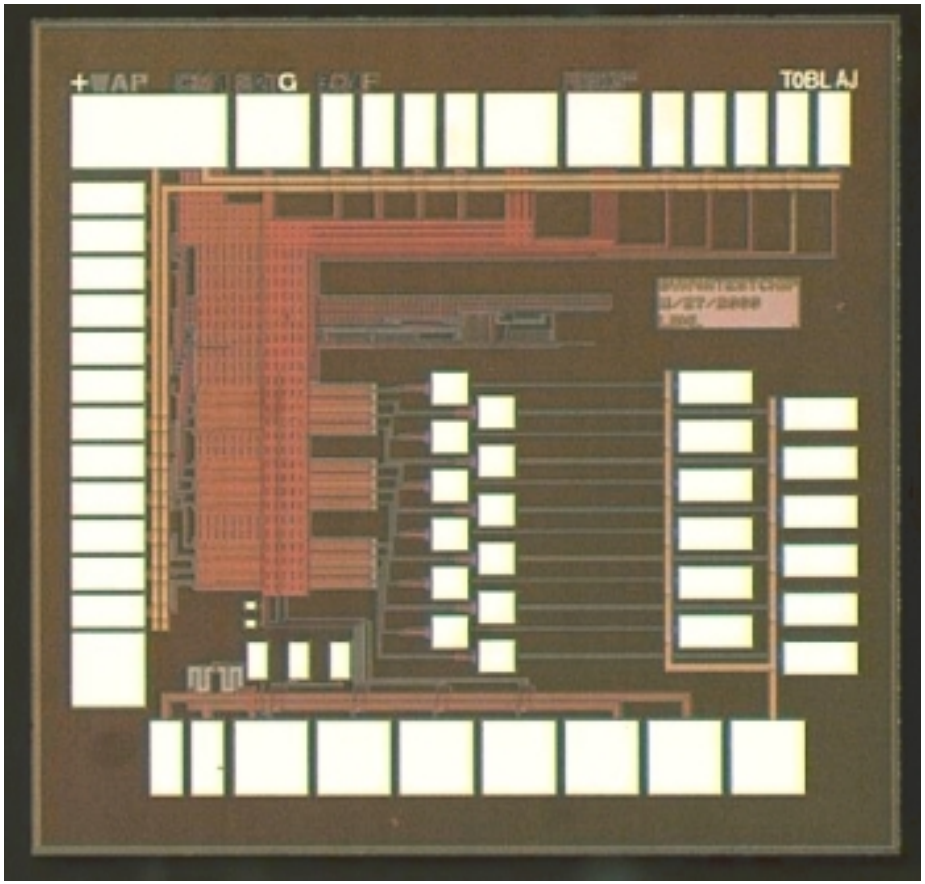
- The outer layer system is rapidly approaching an engineered design
  - ➢ Specify sensors this summer, place order in October for winter delivery
  - ➢ We will start prototyping mechanical designs this summer

# Innermost Layers



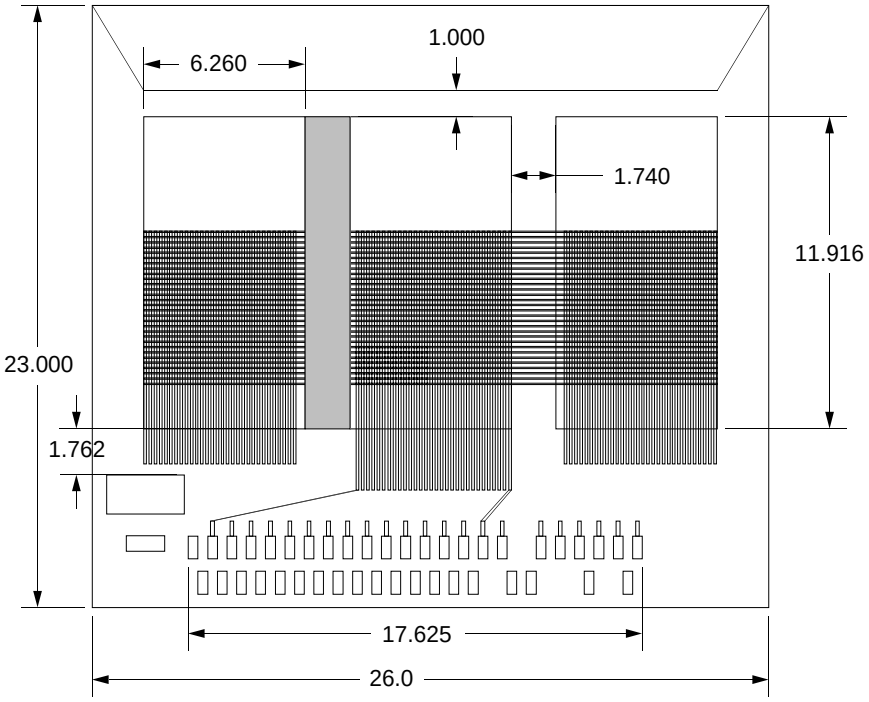
- Plan to rebuild Layer 00
- Studying small radius 90° layer
  - ➢ improved impact parameter resolution in z
    - Does it buy a lot ?
  - ➢ simple $\phi$ segmentation for easier construction
    - Can it be done with low cost and effort ?

# SVX4 Chip



- DØ & CDF - same architecture
- 0.25 μm CMOS
  - rad-hard to > 30 Mrads
  - confidence in simulation models
  - commercial foundries
- TSMC analog test chip received in march
  - Tests agree w/simulation results to better than 10%
    - 1,750e- for 40pF load
- Specifications complete
  - CDF & D0 physicists have agreed upon a detailed list.
    - 1 polarity simplifies design
- Roughly on schedule

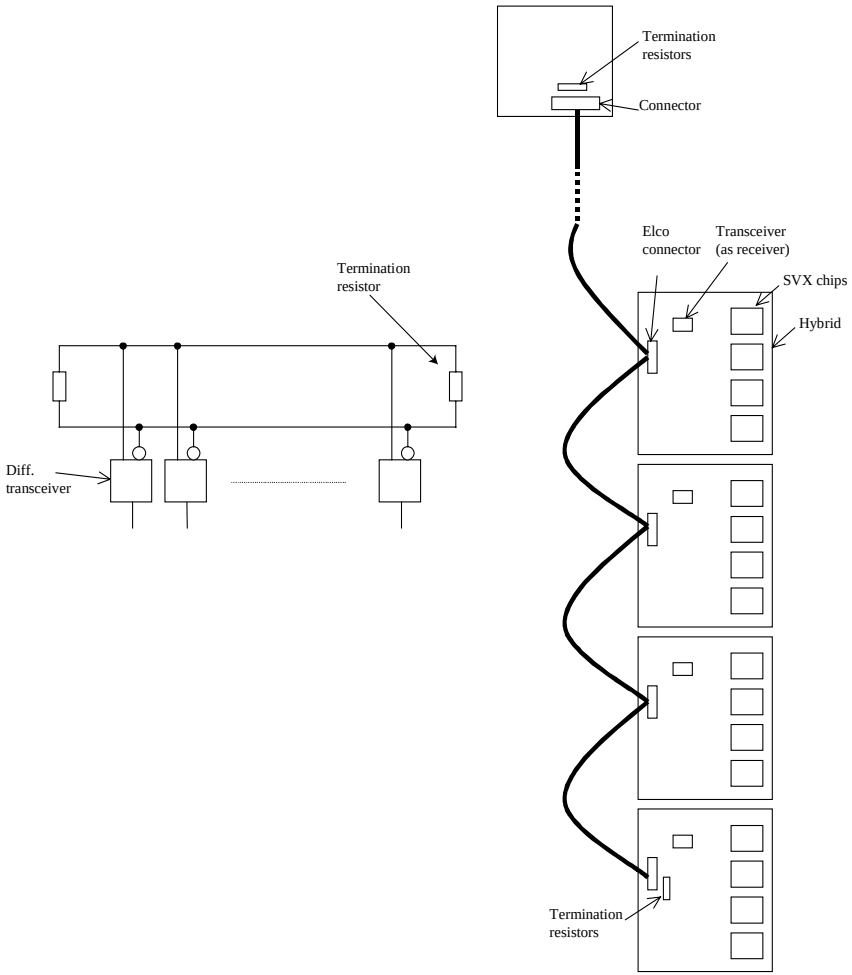
# Hybrids




3 chip hybrid concept
CDF-Run2b SVX-IIB
6/12/2000 C.Haber

- Layer 00 technology
  - Combine screening with etching to achieve high density
  - Smaller more compact hybrids
- Footprint for outer layers done
  - 53.2 mm wide
  - 4 chips
  - $Al_2O_3$ or BeO substrate
    - 0.015-0.025 inches thick
- Inner layer prototypes
  - Same as outer but 2 chips
- Plans
  - Complete layout and prototype this summer using existing SVX3D chips

# DAQ& PS




- DAQ
  - Basic plan
    - Eliminate DOIMs & Merge portcards
    - Gang hybrids as needed
  - Motivation
    - DOIMs are a lot of will die
    - Reduction in complexity
  - Power Supplies
    - Extend support contracts with CAEN.
    - More high bias supplies

# Silicon & Cables

- Silicon
  - 2 mask sets for the outer layers and 2 - 4 sets for inner.
  - No strong need to prototype for radiation testing.
    - LHC has done extensive testing
    - Layer 00 will be a useful gauge
  - Have quotations from HPK.
    - Updating now and negotiating a production schedule
- Lightweight Cables
  - Just received a Layer 00 cable from Keycom (Japan)
    - Even lighter than those in L00
    - Cost looks reasonable
      - 4k$ for masks and $600-700 per sheet (5 cables ?)
      - Now working with Keycom to understand yield and schedule information. (Plan to visit Japan this summer or fall)


# Organization

- Run2b Silicon Leadership and Guidance
  - JI will lead group in CY01
  - Formed internal steering committee of top CDF experts
    - Determine the initial specifications *with emphasis on simplicity for cost and schedule containment*
    - Will review any proposed changes to design
      - Insure that we do not complicate the design for small improvements.
  - Two group co-leaders being sought now.
    - Will work with JI this year and take over in CY02

# R&D/Prototyping

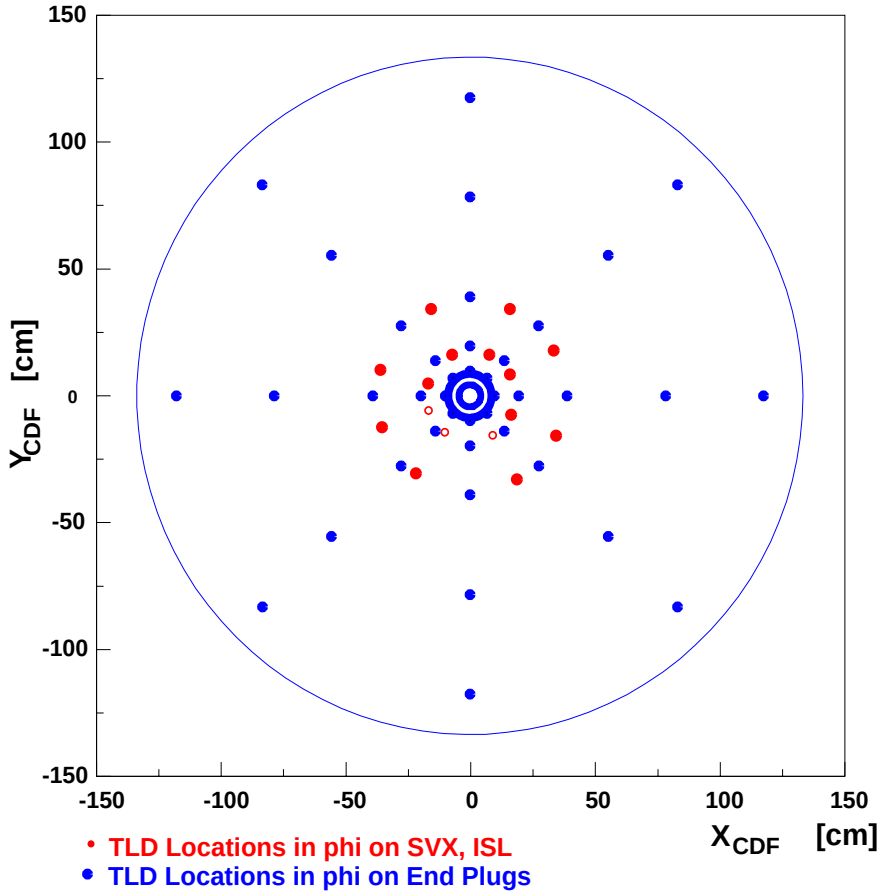
- Plan to build a few ladders
  - Silicon (existing L00 or LHC)
  - Lightweight signal cable (have prototype L00 from Keycom)
  - Hybrid with existing chips (this summer/fall)
  - Mechanical support (design in progress)
- Plug into existing DAQ with “Run 2b Configuration”
  - Mother cable/board from hybrid to HDI (conceptual design)
  - Mini-portcard (design in progress)
  - Long HDI (existing ISL)
  - “Port-card” (existing)
- Resolves almost every open issue

# Design Finalization

- Performance Studies in progress
  - For June PAC: Basic information studies, including ghosting, resolutions, material effects
  - For Autumn TDR: Pattern recognition, object identification, physics impact

- Autumn: Targets
  - Better understanding of Run 2a performance, lifetimes
  - Fully optimized design with physics justification
  - Detailed initial designs of all components
  - Prototype results for critical components
  - Complete resource loaded schedule: all costs, cost bases, contingency analysis

# Radiation Monitoring




- Run 2a Dosimetry
  - Cross-check other monitors
  - Predict damage profiles
- Positioning
  - A fairly extensive system of monitors now in place
  - Based on toy study with 3 source components: Uniform in space, Cylindrically Symmetric about beam, Spherically symmetric about IP
- Status
  - Mylar leaders installed
  - Calibrations complete
  - Holders loaded
  - TLDs to be pulled later this year – should help us understand our dose rates

# Preliminary Cost Estimates

| Item | Estimated Cost [k$] | Contingency [k$] | Total Cost [k$] |
|---|---|---|---|
| SVX4* | 150 | 75 | 225 |
| Silicon | 800 | 400 | 1200 |
| Signal Cables | 300 | 200 | 500 |
| Hybrids | 700 | 350 | 1050 |
| Power Supplies & Crates | 300 | 200 | 500 |
| HDIs | 150 | 75 | 225 |
| P/J Cards | 400 | 300 | 700 |
| Beam pipe | 200 | 100 | 300 |
| Mechanics & Cooling | 600 | 400 | 1000 |
| *TOTAL M&S* | 3,600 | 2,100 | 5,700 |

- Estimates (expected to change)
  - Silicon, Hybrids, Signal Cables, SVX4 costs reasonably well understood
  - Other estimates uncertain and will be refined in upcoming weeks
- Additional Funding sources
  - Japanese will contribute strongly to Silicon and Signal Cables
  - Hope for Italian help on Power Supplies, SVX4 and Silicon
  - University support in FY01 for R&D (see next page)

* Assumes half of the SVX4 chip cost is accounted by D0

# FY01 R&D

| Item | Estimated Cost [k$] | US Cost [k$] |
|---|---|---|
| SVX4* | ? | ? |
| Silicon | 0 | 0 |
| Signal Cables | 40 | 0 |
| Hybrids & Cables | 40 | 40 |
| Power Supplies & Crates | 0 | 0 |
| P/J Cards | 40 | 40 |
| Beam pipe | 0 | 0 |
| Mechanics & Cooling | 50 | 50 |
| *TOTAL M&S* | 170 | 130 |

- Rough Estimates
- University funds may be available
- Does not include SVX4 development costs


# Summary

- Will replace SVXII and L00
- Run 2b system will be simple, robust and powerful
  - Eliminate port-cards
  - Single sided silicon and lightweight signal cables
  - Factor of 2 reduction in material in tracking region
  - Performance & acceptance expected to improve
  - 3D vertexing under study
- Focus on simplicity
  - Cost and schedule containment
- Minimal R&D
- Target:
  - Design by end of FY01
  - Start production in FY02

# Quantities and Costs

| Layout Table | Phi Modularity | | Length | Sensor Length | Z Modularity | Axial Radius | Stereo Radius | Stereo | Channels |
|---|---|---|---|---|---|---|---|---|---|
| Layer | Axial | Stereo | [mm] | [mm] | | [mm] | [mm] | Config | |
| 5 | 24 | 24 | 1200 | 100 | 12 | 170 | 160 | shallow | 147456 |
| 4 | 18 | 18 | 1200 | 100 | 12 | 130 | 125 | shallow | 110592 |
| 3 | 12 | 12 | 1200 | 100 | 12 | 95 | 90 | shallow | 73728 |
| 2 | 18 | 12 | 1000 | 83 | 12 | 55 | 60 | shallow or 90 | 92160 |
| 1 | 12 | 8 | 1000 | 83 | 12 | 35 | 40 | shallow or 90 | 61440 |
| 0 | 12 | 6 | 800 | 66 | 12 | 15 | 20 | 90 or none | 55296 |

| | Totals | | | | | |
|---|---|---|---|---|---|---|
| | **Outer** | **Inner** | **L00** | **All** | **Chips** | **Channels** |
| **Sensors** | 1424 | 690 | 280 | 2394 | 4224 | 540672 |
| **Area [m^2]** | 7.55 | 1.72 | 0.28 | 9.54 | | |

| Installed Quantities | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | A2 sensors | A1 Sensors | A0 Sensors | S2 Sensors | S1 Sensors | S0 Sensors | Chips | 4 chip | 2 chip | mini-pc | hdi-sets | jp card | ftm mods |
| 5 | 288 | | | 288 | | | 1152 | 288 | | 72 | 72 | 14 | 70 |
| 4 | 216 | | | 216 | | | 864 | 216 | | 54 | 54 | 11 | 55 |
| 3 | 144 | | | 144 | | | 576 | 144 | | 36 | 36 | 7 | 35 |
| 2 | | 216 | | | 144 | | 720 | | 336 | 42 | 42 | 8 | 40 |
| 1 | | 144 | | | 96 | | 480 | | 168 | 28 | 28 | 6 | 30 |
| 0 | | | 144 | | | 72 | 432 | | 216 | 54 | 54 | 11 | 55 |
| Installed quantities | 648 | 360 | 144 | 648 | 240 | 72 | 4224 | 648 | 720 | 286 | 286 | 57 | 285 |
| Spare % | 0.1 | 0.15 | 0.3 | 0.1 | 0.15 | 0.3 | 0.5 | 0.1 | 0.1 | 0.3 | 0.3 | 0.2 | 0.2 |
| Total Purchased | 712 | 414 | 187 | 712 | 276 | 93 | 6336 | 712 | 792 | 371 | 371 | 68 | 342 |
| Estimated Unit Cost | 475 | 275 | 275 | 475 | 533 | 533 | 35 | 600 | 400 | 265 | 300 | 300 | 265 |
| Total Cost | 338200 | 113850 | 51425 | 338200 | 147200 | 49600 | 221760 | 427200 | 316800 | 98315 | 111300 | 20400 | 90630 |

# More Details

| SIGNAL CABLES | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | W5 | W4 | W3 | W2 | W1 | W0 | N5 | N4 | N3 | N2 | N1 | N0 | |
| 5 | | 96 | | 96 | | 96 | | | | | | | |
| 4 | | 72 | | 72 | | 72 | | | | | | | |
| 3 | | 48 | | 48 | | 48 | | | | | | | |
| 2 | | | | | | | 48 | 120 | 48 | 120 | 48 | 120 | |
| 1 | | | | | | | 32 | 80 | 32 | 80 | 32 | 80 | |
| 0 | | | | | | | 24 | 72 | 24 | 72 | 24 | 72 | |
| Installed | | 216 | | 216 | | 216 | 104 | 272 | 104 | 272 | 104 | 272 | |
| Spare % | | 50% | | 50% | | 50% | 50% | 50% | 50% | 50% | 50% | 50% | |
| Total Purchased | | 324 | | 324 | | 324 | 156 | 408 | 156 | 408 | 156 | 408 | |
| Est. Unit Cost | | $333 | | $166 | | $66 | $133 | $133 | $111 | $111 | $83 | $66 | |
| Total Cost | | $107,892 | | $53,784 | | $21,384 | $20,748 | $54,264 | $17,316 | $45,288 | $12,948 | $26,928 | $360,552 |

# Cost Estimate

| TOTALS | | | |
|---|---|---|---|
| **Item** | **Cost** | **Contingency** | **Sum** |
| **Sensors** | 1,038,475 | 519,238 | 1,557,713 |
| **Chips** | 221,760 | 110,880 | 332,640 |
| **2 Chip Hybrids** | 316,800 | 158,400 | 475,200 |
| **4 Chip Hybrids** | 427,200 | 213,600 | 640,800 |
| **mini-pc** | 98,315 | 49,158 | 147,473 |
| **hdi sets** | 111,300 | 55,650 | 166,950 |
| **jp Cards** | 20,400 | 10,200 | 30,600 |
| **FTM mods** | 90,630 | 45,315 | 135,945 |
| **Power Supplies & Crates** | 300,000 | 200,000 | 500,000 |
| **Beam pipe** | 200,000 | 100,000 | 300,000 |
| **Mechanics & Cooling** | 600,000 | 400,000 | 1,000,000 |
| **Cables** | 360,552 | 252,386 | 612,938 |
| **Totals** | **3,785,432** | **2,114,826** | **5,900,258** |

- To be a bit more conservative – assume the inner layers are 90 degree stereo double metal detectors

# Conservative Hybrids Model

| Conservative Totals | | | |
|---|---|---|---|
| **Item** | **Cost** | **Contingency** | **Sum** |
| **Sensors** | 1,038,475 | 519,238 | 1,557,713 |
| **Chips** | 221,760 | 110,880 | 332,640 |
| **2 Chip Hybrids** | 553,176 | 165,953 | 719,129 |
| **4 Chip Hybrids** | 732,046 | 219,614 | 951,659 |
| **mini-pc** | 98,315 | 49,158 | 147,473 |
| **hdi sets** | 111,300 | 55,650 | 166,950 |
| **jp Cards** | 20,400 | 10,200 | 30,600 |
| **FTM mods** | 90,630 | 45,315 | 135,945 |
| **Power Supplies & Crates** | 300,000 | 200,000 | 500,000 |
| **Beam pipe** | 200,000 | 100,000 | 300,000 |
| **Mechanics & Cooling** | 600,000 | 400,000 | 1,000,000 |
| **Cables** | 360,552 | 252,386 | 612,938 |
| **Totals** | **4,326,654** | **2,128,393** | **6,455,046** |

# Cost Basis

- Vendor quotes in many cases or used Run 2a costs
  - Silicon – HPK quote
  - Hybrids – LBL experience in Run 2a + Vendor quotes for substrates
  - Cables – quote from Keycom Corp. (NRE in contingency)
  - HDIs- Based on actual cost of ISL 1.2 m long HDIs
    - served similar purpose but twice as long as those for Run 2b
  - Other DAQ items estimated by FNAL Electronics group
  - Beampipe estimate with contingency is twice the Run 2a cost
  - Power supplies based on Run 2a ISL and L00 supply & crate costs
  - SVX4 cost is only for final CDF production run. It does not include the NRE costs being incurred in the joint SVX4 design project.
- 50-70% contingency on all tasks

# Comments

- Areas where we are uncertain
  - Signal Cables (but we assumed 50% yield and 50% contingency)
  - Mechanics & Cooling (assumed 600k$ and 400k$ contingency)
    - No Beryllium parts
    - Simple low mass cylinders and support flanges
    - Limited fixturing
      - Can re-use all of our installation fixtures for installation in ISL
    - Don't know if we will need to increase the capacity of our chiller plant
      - Chillers are around 10k$. The whole system is of order 100k$ ?
- We'll refine this somewhat over the next month
  - Mainly work on signal cables and mechanics costs.
  - Update quotes on silicon
  - Try to make up some things…